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| 09/937,468 | 09/25/2001 | Timothy Heighway | PD990017 | 9487 |

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| EXAMINER | |
|---|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2112 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/937,468 | HEIGHWAY ET AL. | |
| | Examiner | Art Unit | |
| | Christopher E. Lee | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27* is/are allowed.

6)☒ Claim(s) *1,4-12,15-19 and 21-26* is/are rejected.

7)☒ Claim(s) *2,3,13,14 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Receipt Acknowledgement*

1. Receipt is acknowledged of the request filed on 24th of February 2005 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/937,468, which the request is acceptable and an RCE has been established. Claims 1-9, 15 and 18 have been amended; no claim has been canceled; and claims 24-27 have been newly added since the Final Office Action was mailed on 19th of November 2004. Currently, claims 1-27 are pending in this application.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 8, 25 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim 8 recites the limitation "the beginning of the next free location" in line 8. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "the beginning of the next free location" could be considered as --a beginning of a next free location-- since it is not clearly defined in the claims.

The claim 25 recites the limitation "the isochronous data format header" in line 4. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "the isochronous data format header" could be considered as --an isochronous data format header-- since it is not clearly defined in the claims.

The claim 26 recites the limitation "the first data block" in line 6. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "the first data block" could be considered as --a first data block-- since it is not clearly defined in the claims.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 4, 6, 7, 9-11, 15, 18, 19, 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Bunting et al. [WO 95/15651; hereinafter Bunting].

*Referring to claim 1,* Bunting discloses a method for assembling data packets (See page 1, lines 5-9) for isochronous data transmission (See page 4, lines 7-17; i.e., wherein in fact that input processor unit includes a signal delay network for processing the picture start code-word and the PAP so that the PAF occurs in the code word clock cycle immediately before the I frame picture start codeword, and the delay network assures that the output signals applied to packed word controller unit and data packer unit exhibit proper time synchronism inherently anticipates that said data packets are for isochronous data transmission) via a data bus (i.e., via Transmission Channel in Fig. 19), a data format for said isochronous data transmission being defined in an isochronous data format header of said data packet (See page 5, line 29 through page 6, line 2; i.e., wherein in fact that each header contains information related to the data in the data packet with which the header is associated, and the header information aids data assembly and synchronization at a receiver, and includes information such as service type, frame type, frame number and slice number inherently anticipates that a data format for said isochronous data transmission is defined in an isochronous data format header of said data packet), comprising the steps of: writing said isochronous data format header to a special register (i.e., Output Register 78 of Fig. 17) and to a buffer memory (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714, shown in Fig. 17) for said data packets (i.e., in fact, Header is written to said Header FIFO and also written to said Output Register and said Rate Buffers in the form of being combined with Data) when

said isochronous data transmission is set up in a data transmitting device (i.e., setting up in a video signal encoder; See page 2, lines 27-30, and page 3, lines 30+); and attaching (i.e., combining) useful data of said data packet (i.e., packed data words) to said isochronous data format header (i.e., Header) in said buffer memory (i.e., combining Data from said Data FIFO with Header in said Header FIFO are stored in said Output Register and said Rate Buffers; See page 5, lines 11-28); and taking both said isochronous data format header and said useful data from said buffer memory for data transmission (See page 19, lines 3-15).

*Referring to claim 4,* Bunting teaches selecting same number of data blocks per data packet (See page 3, lines 30-34; i.e., wherein in fact that 960 bits per data packets anticipates selecting same number of data blocks per data packet).

*Referring to claim 6,* Bunting discloses an apparatus (i.e., video signal encoder in Fig. 1) for carrying out said method according to claim 1 (See claim 1 rejection), comprising a buffer memory for data packets (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714, shown in Fig. 17), having a special register (i.e., Output Register 78 of Fig. 17) for said isochronous data format header (i.e., Header) of one of said data packets (i.e., Output Register 78 including said Header in the form of being combined with Data in Fig. 17), and having initialization means (i.e., FIFO State Controller 74 and Header/Data Multiplexer 76 in Fig. 17), which copy said isochronous data format header for a first data packet of said isochronous data transmission to said special register for said isochronous data format header and said buffer memory (See page 14, lines 19+; i.e., copying Header for data packet word of isochronous data transmission to Output Register for combining said Header, and being stored in said Rate Buffers 713 and 714 in Fig. 19), and transmission means (i.e., Modem 717 of Fig. 19) for reading (i.e., retrieving and transmitting) both said isochronous data format header and said useful data from said buffer memory for data transmission (See page 19, lines 3-15).

*Referring to claim 7,* Bunting teaches said isochronous data format header (i.e., Header) for said first data packet is prescribed for said initialization means (i.e., said Header is generated by Header Generator 18 of Fig 1 for said FIFO State Controller 74 and Header/Data Multiplexer 76 in Fig. 17) by an application process (i.e., by digital television signal processing; See Abstract).

*Referring to claim 9,* Bunting discloses a method for assembling data packets for data transmission (See page 1, lines 5-9) via a data bus (i.e., via Transmission Channel in Fig. 19), said method comprising: writing a data header (i.e., Header) to a special register (i.e., Output Register 78 of Fig. 17) and to a selected portion (i.e., Header FIFO 70 of Fig. 17) of a buffer memory for said data packets (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714, shown in Fig. 17); and appending (i.e., combining) useful data in a form of data blocks (i.e., packed data words) to said data header (i.e., Header) located in said buffer memory (i.e., combining Data from said Data FIFO with Header in said Header FIFO are stored in said Rate Buffers; See page 5, lines 11-28); and taking both said isochronous data format header and said useful data from said buffer memory for data transmission (See page 19, lines 3-15).

*Referring to claim 15,* Bunting teaches selecting a same number of data blocks per data packet (See page 3, lines 30-34; i.e., wherein in fact that 960 bits per data packets anticipates selecting same number of data blocks per data packet).

*Referring to claim 18,* Bunting discloses an apparatus (i.e., video signal encoder in Fig. 1) for assembling data packets for data transmission (See page 1, lines 5-9) via a data bus (i.e., via Transmission Channel in Fig. 19), comprising: a buffer memory (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714, shown in Fig. 17) for said assembly of data packets (i.e., combining Header and Data; See page 14, lines 27-33); a special register (i.e., Output Register 78 of Fig. 17) for storing a data header (i.e., Header) of a first one of said data packets (i.e., Output Register 78 including said Header in the form of being combined with Data in Fig. 17); and an initialization means

(i.e., FIFO State Controller 74 and Header/Data Multiplexer 76 in Fig. 17) for copying said data header for said first data packet to said special register and to said buffer memory (See page 14, lines 19+; i.e., copying Header for data packet word of isochronous data transmission to Output Register for combining said Header, and being stored in said Rate Buffers 713 and 714 in Fig. 19); and transmission means (i.e., Modem 717 of Fig. 19) for reading (i.e., retrieving and transmitting) both said isochronous data format header and said useful data from said buffer memory for data transmission (See page 19, lines 3-15).

*Referring to claim 19,* Bunting teaches said data header (i.e., Header) for said first data packet is prescribed by an application process (i.e., said Header is generated by Header Generator 18 of Fig 1 for said FIFO State Controller 74 and Header/Data Multiplexer 76 in Fig. 17 of digital television signal processing; See Abstract).

*Referring to claims 10, 11, 21 and 22,* Bunting teaches said data packets are isochronous data packets, and said data bus is an isochronous data bus (See page 4, lines 7-17; i.e., wherein in fact that input processor unit includes a signal delay network for processing the picture start code-word and the PAP so that the PAF occurs in the code word clock cycle immediately before the I frame picture start codeword, and the delay network assures that the output signals applied to packed word controller unit and data packer unit exhibit proper time synchronism inherently anticipates that said data packets are isochronous data packets, and said data bus is an isochronous data bus).

***Claim Rejections - 35 USC § 103***

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 5, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunting [WO 95/15651] as applied claims 1, 4, 6, 7, 9-11, 15, 18, 19, 21 and 22 above, and further in view of what was well known in the art, as exemplified by Takayama [US 5,991,842 A].

*Referring to claims 5, 16 and 17,* Bunting discloses all the limitations of the claims 5, 16 and 17, respectively, except that does not teach dividing said data to be transmitted into data source packets, wherein, in particular for said transmission of MPEG2 video data, a data source packet is composed from 8 data blocks.

The Examiner takes Official Notice that dividing said data to be transmitted into data source packets, wherein, in particular for said transmission of MPEG2 video data, a data source packet is composed from 8 data blocks, is well known to one of ordinary skill in the art, as evidenced by Takayama (See col. 9, lines 33-44).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have applied said method step of dividing said data source packets into 8 data blocks, as disclosed by Takayama, to said method, as disclosed by Bunting, since it would have ensured a communications being performed by using said data bus (i.e. 1394 serial bus) at a predetermined communication cycle (See Takayama, Fig. 6 and col. 5, lines 24-31).

8. Claims 12 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunting [WO 95/15651] as applied claims 1, 4, 6, 7, 9-11, 15, 18, 19, 21 and 22 above, and further in view of Sato et al. [US 6,259,694 B1; hereinafter Sato].

*Referring to claims 12 and 23,* Bunting discloses all the limitations of the claims 12 and 23, respectively, except that does not teach said data header comprising a comparison value for counting data blocks.

Sato discloses a method of enabling an error bit to be set simply without causing an increase in the size of signal processing circuit (See Abstract), wherein a data header (i.e., CIP Header in Fig. 14) comprising a comparison value (i.e., data block continuity counting value in DBC field of Fig. 14) for counting data blocks (i.e., detecting the number of the isochronous packets; See col. 10, lines 54-55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said comparison value for counting data blocks (i.e., DBC field), as disclosed by Sato, in said data header, as disclosed by Bunting, for the advantage of indicating discontinuity when it detects the discontinuity of the DBC (i.e., indicating packet loss; See Sato, col. 10, line 66 through col. 11, line 6).

9. Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunting [WO 95/15651] in view of Sato [US 6,259,694 B1].

*Referring to claim 24,* Bunting discloses a method for assembling data packets (See page 1, lines 5-9) for isochronous data transmission (See page 4, lines 7-17; i.e., wherein in fact that input processor unit includes a signal delay network for processing the picture start code-word and the PAP so that the PAF occurs in the code word clock cycle immediately before the I frame picture start codeword, and the delay network assures that the output signals applied to packed word controller unit and data packer unit exhibit proper time synchronism inherently anticipates that said data packets are for isochronous data transmission) via a data bus (i.e., via Transmission Channel in Fig. 19), a data format for said isochronous data transmission being defined in an isochronous data format header of a bus packet (See page 5, line 29 through page 6, line 2; i.e., wherein in fact that each header contains information related to the data in the data packet with which the header is associated, and the header information aids data assembly and synchronization at a receiver, and includes information such as service type, frame type, frame number and slice number inherently anticipates that a data format for said isochronous data transmission is defined in an isochronous data format header of a bus packet), comprising the steps of: writing said isochronous data format header to a special register (i.e., Output Register 78 of Fig. 17) and to a buffer memory (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714, shown in Fig. 17) for said data packets (i.e., in fact, Header is written to said Header FIFO and also written to said Output Register and said Rate Buffers in the form of being combined with Data) when

said isochronous data transmission is set up in a data transmitting device (i.e., setting up in a video signal encoder; See page 2, lines 27-30, and page 3, lines 30+); and attaching (i.e., combining) useful data of said data packet (i.e., packed data words) to said isochronous data format header (i.e., Header) in said buffer memory (i.e., combining Data from said Data FIFO with Header in said Header FIFO are stored in said Output Register and said Rate Buffers; See page 5, lines 11-28).

Bunting does not teach said isochronous data format header including a comparison value generated by a data block counter for data block counting.

Sato discloses a method of enabling an error bit to be set simply without causing an increase in the size of signal processing circuit (See Abstract), wherein an isochronous data format header (i.e., CIP Header in Fig. 14) including a comparison value (i.e., data block continuity counting value in DBC field of Fig. 14) generated by a data block counter (i.e., counter for detecting the number of the isochronous packets) for data block counting (i.e., detecting the number of the isochronous packets; See col. 10, lines 54-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said comparison value for data block counting (i.e., DBC field), as disclosed by Sato, in said data header, as disclosed by Bunting, for the advantage of indicating discontinuity when it detects the discontinuity of the DBC (i.e., indicating packet loss; See Sato, col. 10, line 66 through col. 11, line 6).

*Referring to claim 26,* Bunting discloses a method for assembling data packets for data transmission (See page 1, lines 5-9) via a data bus (i.e., via Transmission Channel in Fig. 19), said method comprising: writing a data header (i.e., Header) to a special register (i.e., Output Register 78 of Fig. 17) and to a selected portion (i.e., Header FIFO 70 of Fig. 17) of a buffer memory for said data packets (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714, shown in Fig. 17); and appending (i.e., combining) useful data in a form of data blocks (i.e., packed data words) to said data header (i.e., Header) located in said buffer memory (i.e., combining Data

from said Data FIFO with Header in said Header FIFO are stored in said Rate Buffers; See page 5, lines 11-28).

Bunting does not teach said data header comprising a comparison value for counting data blocks, said comparison value is a number of data blocks, and said comparison value relates to a first data block in said data packet.

Sato discloses a method of enabling an error bit to be set simply without causing an increase in the size of signal processing circuit (See Abstract), wherein a data header (i.e., CIP Header in Fig. 14) comprising a comparison value (i.e., data block continuity counting value in DBC field of Fig. 14) for counting data blocks (i.e., detecting the number of the isochronous packets; See col. 10, lines 54-55), said comparison value is a number of data blocks (See col. 10, line 55; actually, the number of the isochronous packets in DBC region shows a number of data blocks), and said comparison value relates to a first data block in said data packet (in fact, the number of data blocks in DBC region are in sequence from the first source packet for indicating a potential discontinuity error; See col. 10, line 66 through col. 11, line 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said comparison value for counting data blocks (i.e., DBC field), as disclosed by Sato, in said data header, as disclosed by Bunting, for the advantage of indicating discontinuity when it detects the discontinuity of the DBC (i.e., indicating packet loss; See Sato, col. 10, line 66 through col. 11, line 6).

***Allowable Subject Matter***

10. Claim 27 is allowed.

11. Claims 8 and 25 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. Claim 2, 3, 13, 14 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter:

The limitations of claims 2, 8, 13 and 20 are respectively deemed allowable over the prior art of record as the prior art fails to teach or suggest that updating (transferring) said comparison value in said data header in said special register when said useful data in data blocks are written to said buffer memory, and copying said updated data header to said buffer memory at a next free location for a data packet in said buffer memory. The claim 3 is a dependent claim of the claim 2, and the claim 14 is a dependent claim of the claim 13.

The limitations of claim 25 is deemed allowable over the prior art of record as the prior art fails to teach or suggest that a memory management unit transfers a counter reading of the data block counter after the counting of the data blocks of said one of said data packets to the isochronous data format header stored in the special register, and copies the isochronous data format header that has been updated in this way in the special register to the buffer memory at the beginning of the next free location for said one of said data packets.

The limitations of claim 27 is deemed allowable over the prior art of record as the prior art fails to teach or suggest that a data block counter transfers a count in said data block counter to said data header stored in said special register, and further wherein said count in said special register is copied to said buffer memory at a next free location.

***Response to Amendment***

14. Regarding to the Applicants' amendment/response filed on 24th of February 2005 (hereinafter the Response), the Examiner notes that the case Serial No. 09/956,332 in the Heading of the paper is not

correct. However, the Examiner presumes the case Serial No: 09/956,332 in the Heading of the paper was incorrect because of a typographical error, and the proposed reply has been entered for consideration.

***Response to Arguments***

15. Applicants' arguments filed on 24th of February 2005 have been fully considered but they are not persuasive.

*In response to the Applicant's response with respect to* "Claim 20 is nowhere rejected and is, therefore, assumed to be allowable." on the Response page 8, lines 13-14, the Examiner believes that the Applicants misinterpret the claim 20 objection.

In the Office Action mailed on 19th of November 2004, on page 10, paragraph 12, the Examiner clearly states that the claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

*In response to the Applicants' arguments with respect to* "In sharp contrast, Bunting describes joining data with a packet alignment flag (PAF) using a data/header combiner circuit 15, which includes a data FIFO 16 and a header FIFO 17 ... It can be clearly seen from Fig. 17 and col. 8, lines 9-39 that the data/header combiner 15 of Bunting includes separate data and header FIFOs (72 and 70 respectively) and a multiplexer 76 (e.g., selection logic unit). It is respectfully submitted that, in fact, Bunting teaches away from the present invention. As recited in independent claim 1, both the isochronous data format header and the payload (useful data) are taken from a buffer in which the packet is already formed in the right format. It is further respectfully submitted that the present invention is, therefore, not anticipated and is patentable over Bunting." on the Response page 9, lines 15-25, the Examiner notices that the arguments are drawn to the amended limitations which have not been considered. However, in contrary to the Applicants' statement, Bunting still suggests the amended limitations in the claimed invention (See

paragraph 5 of the instant Office Action, Claims 1, 4, 6, 7, 9-11, 15, 18, 19, 21 and 22 rejection under 35 U.S.C. 102(b) as being anticipated by Bunting).

Thus, the Applicants' arguments on this point is not persuasive.

*In response to the Applicants' arguments with respect to* "Regarding claims 12 and 23, Sato describes in detail the isochronous cycle of a IEEE 1394 bus inclusive of the isochronous bus packet format and the late check (error bit). Sato also describes at col. 10, line 35 to 40 that the post-transmission circuit 107 adds the 1394 header and CIP header to the data containing a source packet header stored in the FIFO. Data flow in Fig. 5 is from FIFO 110 to Link Core 101 via post processing unit 107. The CIP header is added to the source packet 'On the Fly'. This teaches away from the present invention in which both the CIP header and the source packet data is taken/read from the buffer memory." on the Response page 10, lines 5-12, the Examiner respectfully disagrees.

Actually, the newly added limitation, i.e., taking both said isochronous data format header and said useful data from said buffer memory for data transmission, is suggested by Bunting, page 19, lines 3-15. Sato is suggesting the limitation "said data header comprising a comparison value for counting data blocks." Therefore, the combination of Bunting and Sato with rationale for the proper combining suggests the obviousness of the claimed invention.

Furthermore, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Thus, the Applicants' arguments on this point is not persuasive.

***Conclusion***

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

cel/ CEL

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100